7 Memory

7.1 Overview

The PowerEdge R710 uses DDR3 memory, providing a high-performance, high-speed memory interface capable of low latency response and high throughput. The R710 supports Registered ECC DDR3 DIMMs (RDIMM) or Unbuffered ECC DDR3 DIMMs (UDIMM).

The system contains 18 memory sockets split into two sets of nine sockets, one set for each processor. Each nine-socket set is organized into three channels of three memory sockets per channel.

Key features of the R710 memory system include the following:

- Registered (RDIMM) and Unbuffered (UDIMM) ECC DDR3 technology
- Up to 288 GB of RDIMM memory (eighteen 16 GB dual rank RDIMMs)
- Up to 24 GB of UDIMM memory (twelve 2 GB UDIMMs)
- Support for 1066/1333 MHz single- and dual-rank DIMMs
- Support for 1066 MHz quad-rank DIMMs
- Support for 1.35V low voltage (LV) DIMMs with 5600 series processors
- 64 data and eight ECC bits per channel
- Support for single DIMM configuration (DIMM in socket A1 only)
- Support for ODT (On Die Termination) clock gating (CKE) to conserve power when DIMMs are not accessed (DIMMs enter a low power self-refresh mode)
- I2C access to SPD EEPROM for access to RDIMM thermal sensors
- Single Bit Error Correction
- SDDC (Single Device Data Correction, x4 or x8 devices)
- Support for Closed Loop
- Thermal Management on RDIMMs and UDIMMs
- Multi Bit Error Detection Support for Memory Optimized Mode
- Support for Advanced ECC mode
- Support for Memory Mirroring
- Support for Memory Sparing with 5600 series processors

7.2 DIMMs Supported

The DDR3 memory interface consists of three channels with up to three RDIMMs or two UDIMMs per channel for single or dual rank and up to two RDIMMs per channel for quad rank. The interface uses 2 GB, 4 GB, 8 GB, or 16GB RDIMMs. Also supported are 1 GB or 2 GB UDIMMs.

7.2.1 Memory Modes

The memory mode is dependent on how the memory is populated in the system, according to the following configurations:

- Three channels per processor populated identically
- Dual-processor configuration with the memory configurations for each processor being identical
  - Typically, the system will be set to run in Memory Optimized (Independent Channel) mode in this configuration.
  - This mode offers the most DIMM population flexibility and system memory capacity, but offers the least number of RAS (reliability, availability, service) features.
  - Memory modules are installed in numeric order for the sockets beginning with A1 or B1.

- The first two channels per processor populated identically with the third channel unused
  - Typically, two channels operate in Advanced ECC (Lockstep) mode with each other by having the cache line split across both channels.
  - This mode provides improved RAS features (SDDC support for x8-based memory).
  - For memory mirroring, two channels operate as mirrors of each other (writes go to both channels and reads alternate between the two channels).
  - For Memory Mirroring or Advanced ECC Mode, the three sockets farthest from the processor are unused and memory modules are installed beginning with socket A2 or B2, proceeding in the following order: A2, A3, A5, and A6.
- One channel per processor populated
  - This is a simple Memory Optimized mode.
  - Mirroring is not supported.

7.2.2 DIMM Population Rules

The following DIMM population rules apply:

- If DIMMs of different speeds are mixed, all channels will operate at the fastest common frequency. RDIMMs and UDIMMs cannot be mixed.
- If memory mirroring is enabled, identical DIMMs must be installed in the same slots across both channels.
- The third channel of each processor is unavailable for memory mirroring.
- The R710 memory system supports up to 18 DIMMs. DIMMs must be installed in each channel starting with the DIMM farthest from the processor. Population order is identified by the silkscreen designator and the System Information Label (SIL) located on the chassis cover.

DIMM slot population for each memory mode is listed as follows:

- Memory Optimized: [1, 2, 3], [4, 5, 6], [7, 8, 9]
- Advanced ECC or Mirrored: [2, 3], [5, 6], [8, 9]
- Quad Rank or UDIMM: [1,2,3], [4,5,6]

See the figure below for the layout of the R710 memory channels.

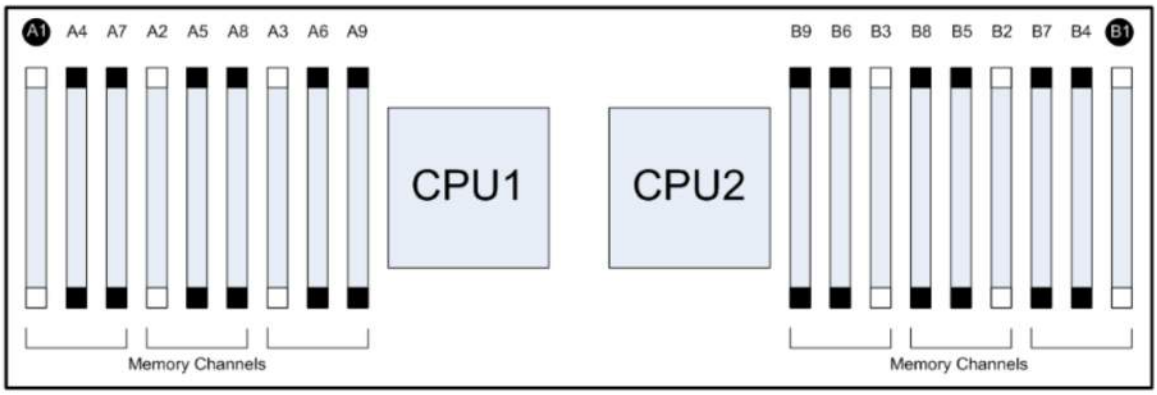

Figure 10. Memory Channels

7.3 Speed

The memory frequency is determined by a variety of inputs:

- Speed of the DIMMs
- Speed supported by the processor
- Configuration of the DIMMs

The memory speed of each channel depends on the memory configuration:

- For single- or dual-rank memory modules:
  - One memory module per channel supports up to 1333 MHz
  - Two memory modules per channel support up to 1066 MHz
  - Three memory modules per channel are limited to 800 MHz, regardless of the memory module speed
- For quad-rank memory modules:
  - One memory module per channel supports up to 1066 MHz
  - Two memory modules per channel are limited to 800 MHz, regardless of memory module speed

If memory modules with different speeds are installed, they will operate at the speed of the slowest installed memory module(s).

7.4 DIMM Slots

The PowerEdge R710 has 18 DIMM slots for memory. It does not have any riser cards for DIMM population.

The first DIMM slot in each channel is color-coded with white ejection tabs for ease of installation. The DIMM sockets are placed 450 mils (11.43 mm) apart, center-to-center to provide enough space for sufficient airflow to cool stacked DIMMs.

7.5 Low Voltage DIMMs

With the introduction of the Intel® Xeon® processor 5600 series, low voltage (LV) DIMMs have been added in selected memory configurations for the PowerEdge R710. Only this processor series supports operating DIMMs at the lower voltage (1.35V, also referred to as DDR3L). The Intel Xeon 5500 processor series does not support low voltage operation. However, due to the backwards-compatible nature of low voltage DIMMs, they can be operated at 1.5V. Therefore, DDR3L DIMMs can be used in systems with either processor series, and the platform will automatically choose the appropriate operating voltage based on the processor populated. DDR3L DIMMs will be qualified and available for use with Intel Xeon 5500 processor series mid-year 2011. Contact your Dell Sales Representative or visit Dell.com for more information.

LV DIMMs operate at 1.35V, creating power savings vs. standard memory which operates at 1.5V. In order to achieve power savings, all DIMMs in the system must be of the LV type. If the system detects a mixture of standard and LV DIMMs, the BIOS will operate all memory at 1.5V. When operating at the lower voltage, additional frequency and population restrictions can take effect. For example, 3 DIMMs per channel operation is not supported at low voltage.

The DDR3L standard is completely backwards-compatible at standard voltage. DDR3L DIMMs can operate at 1.5V without any limitations beyond standard voltage DDR3 DIMMs. As part of the addition of LV DIMMs, the platform has certain default behaviors. Whenever possible, if there is no performance degradation, the platform will default to 1.35V operation when using DDR3L DIMMs. In certain cases, where a configuration is populated that cannot support 1.35V or a performance degradation would result, the platform defaults to 1.5V operation. There are also options to override default voltage within allowed limits.

7.6 Mirroring

The R710 system supports memory mirroring if identical memory modules are installed in the two channels closest to the processor (memory not installed in the farthest channel). Mirroring must be enabled in the System Setup program. In a mirrored configuration, the total available system memory is one-half of the total installed physical memory.

7.7 Sparing

Systems with the Intel Xeon processor 5600 series support memory sparing. Sparing requires identical memory installed in all three channels. One of the three channels is considered the Spare Channel, and two-thirds of the total installed memory is usable and is the amount reported during POST and in BIOS setup.

7.8 Memory Scrubbing

The PowerEdge R710 memory interface supports memory demand and patrol scrubbing, single-bit correction and multi-bit error detection. Correction of a x4 or x8 device failure is also possible with SDDC in the Advanced ECC mode. Additionally, correction of a x4 device failure is possible in the Memory Optimized mode.

7.9 Advanced ECC (Lockstep) Mode

In Advanced ECC (Lockstep) mode, the two channels closest to the processor are combined to form one 128-bit channel. This mode supports Single Device Data Correction (SDDC) for both x4- and x8-based memory modules. Memory modules must be identical in size, speed and technology in corresponding slots.

7.10 Optimizer (Independent Channel) Mode

In Optimizer (Independent Channel) mode, all three channels are populated with identical memory modules. This mode permits a larger total memory capacity but does not support SDDC with x8-based memory modules.

A minimal single-channel configuration of 1 GB memory modules per processor is also supported in this mode.

7.11 Supported Configurations

See the System Memory section in the Installing System Components chapter in the *Dell PowerEdge R710 Systems Hardware Owner's Manual* on Support.dell.com.